THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte XIAO B. ZHANG

Appeal No. 96-0506
Application 07/856,001[1]

ON BRIEF

Before KRASS, JERRY SMITH, and BARRETT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed March 20, 1992, entitled "Process for Independently Protecting Two Dimensional Codes from One or More Burst Error Patterns."

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-10, all the claims pending in the application. In the Examiner's Answer, the examiner maintained the provisional obviousness-type double patenting rejection of claims 1-10 over claims 1-4 of Application 07/856,002 because that application had not yet been abandoned. Since the status of 07/856,002 is now abandoned, it is presumed that the double patenting rejection is now moot. Accordingly, only claims 1-6 stand finally rejected.

The disclosed invention is directed to a method for reading and writing a two-dimensional code having parity protection along multiple axes.

Claim 1 is reproduced below.

> 1. In a method for writing and reading a parity protected binary message of predetermined symbol size into and from, respectively, a two dimensional code; the improvement comprising the steps of
>
> padding said message with a predetermined set of constant bit values to provide a first array of bits that is symbol aligned for certain scan patterns, where the only variables are message bits;
>
> reading out said first array in accordance with a predetermined one of said scan patterns to provide a first set of symbols that are a disjoint cover of said array;
>
> computing at least one symbol oriented error correction code on said first array of bits to produce parity symbols for protecting said message against an anticipated burst error pattern;
>
> encoding said message and a selected number of said parity symbols in said code;
>
> decoding said code for recovering decode values for said message and for said parity symbols;
>
> separating the decode values for said message from the decode values for said parity symbols;

padding said message with said predetermined set of constant bit values to provide a second symbol aligned array of bits that is identical to said first array, subject only to any decode errors that may have corrupted said message;

reading out said second array in accordance with said predetermined one of said scan patterns to provide a second set of symbols that are identical to first set of symbols, subject only to any decode errors that may have corrupted said message; and

computing a decode of said error correction code on said second set of symbols and said parity symbols to correct said decode errors if and when possible.

THE REFERENCES

The examiner relies on the following references ("primary" and "secondary" characterizations are by the examiner):

Primary

Okamoto et al. (Okamoto)	4,646,301	February 24, 1987
Chapman	5,181,207	January 19, 1993
	(filed January 28, 1991)	

Secondary

Cerracchio	4,375,101	February 22, 1983
Patel et al. (Patel)	4,745,604	May 17, 1988
Golden	4,868,824	September 19, 1989
Pughe, Jr. et al. (Pughe)	5,226,043	July 6, 1993
	(filed December 27, 1990)	

THE REJECTIONS

Claims 1-6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Okamoto and Chapman. The examiner cites Cerracchio, Patel, Golden, and Pughe as evidence that it was well known in the art to pad bits, but does not include the references in the statement of the rejection. We refer to the Examiner's Answer for the statement of the rejection.

OPINION

We reverse.

Appellant argues that neither Okamoto nor Chapman teaches or suggests the concept of padding bit arrays with bits having constant values as required to symbol align such arrays for plural "scan patterns" (Brief, pages 5-6). The examiner apparently admits that neither Okamoto nor Chapman teaches padding, but states in the response to the arguments section (Examiner's Answer, pages 7-8):

> Appellant has argued that the cited references do not teach padding to provide symbol aligned arrays of bits. However, it is well known in the art to pad bits; it would have been obvious to one of ordinary skill in the art to modify the cited references because one of ordinary skill in the art would have wanted to ensure the correct communication and/or storage of information. For examples of padding of bits/bytes, see the four references included as part of the final action paper #5, mailed 10/7/94.

The examiner does not explain how the general use of padding bits in the prior art suggests or makes obvious the specific padding recited in claim 1. The examiner relies on Cerracchio, Patel, Golden, and Pughe to show padding. However, we cannot consider the merits of these references because they have not been denominated as a part of the rejection. A rejection must expressly mention the references relied on. In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970) ("Where a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including the reference in the statement of the rejection."). Procedural due process and 35 U.S.C. § 132 of the patent statute require that applicants be adequately notified of the reasons for the rejection of claims so that they can decide how to proceed. See In re Ludtke, 441 F.2d 660, 662, 169 USPQ 563, 565 (CCPA 1971). Knowing exactly

what references are being relied on is considered a vital part of the rejection. The examiner's listing of Cerracchio, Patel, Golden, and Pughe as "secondary" references without making them part of the rejection is an attempt to bring the references in through the "backdoor," seemingly to avoid having to label the rejection as a new ground of rejection. Because neither Okamoto nor Chapman disclose padding, the rejection of claims 1-6 is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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) BOARD OF PATENT
JERRY SMITH) APPEALS
Administrative Patent Judge) AND
) INTERFERENCES
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